REMARKS

The instant Amendment is filed in response to the official action dated March 11, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows.

Claims 1-8 are currently pending.

Claims 1-8 stand rejected.

Claims 1-8 have been amended.

The Applicants' Attorney wishes to thank the Examiner for affording him the opportunity to discuss pending issues and possible clarifying amendments to the claims in the telephonic interview that took place on June 15, 2004. The Applicants' Attorney provided the Examiner with a draft amendment under 37 C.F.R. 1.116 prior to the interview. The discussion during the interview focused on proposed amendments to base claim 1 included in the draft amendment under Rule 116. The prior art references discussed during the interview were the U.S. Patents issued to Nakai *et al.* (USP 6,115,728) and Witek *et al.* (USP 5,430,888). The principal arguments presented to the Examiner during the interview are provided below.

Claims 1-8 were rejected by the Examiner under 35 U.S.C. 103(a) as being obvious over Nakai *et al.* in view of Witek *et al.*

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Specifically, the official action indicates that the Nakai reference discloses the claimed subject matter except for the memory store operation that has a unity stride, thereby allowing R butterfly data values to be read from contiguous memory locations each time the R butterfly data values are read from the third memory. The official action further indicates that the Witek reference discloses the operation of storing in a unity stride so that elements are stored contiguously in memory for ease of accessing and loading. The official action concludes that it would have been obvious to one of ordinary skill at the time of the invention to combine the teachings of the Nakai and Witek references to obtain the claimed subject matter. The Applicants respectfully submit, however, that the official action has failed to establish a *prima facie* case of obviousness, and therefore the rejections of the claims under section 103 of the Patent Laws are improper and should be withdrawn.

It is well settled that a *prima facie* case of obviousness is established when the teachings of the prior art references suggest the benefits of combining the references, thereby providing the motivation to one of ordinary skill in the art to make the combination. Because the cited Nakai and Witek references fail to suggest the desirability of combining them, a *prima facie* case of

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obviousness has not been established and therefore the rejections of claims 1-8 under 35 U.S.C. 103 are unwarranted.

Specifically, the instant application addresses problems relating to the computation of Fast Fourier Transforms (FFTs). Like the instant application, the Nakai reference relates to apparatus and methods for performing FFTs. <u>However, the Witek reference has nothing to do with FFTs</u>. Instead, Witek *et al.* address problems relating to loading data from a cache memory to registers (see column 1, lines 12-15, of Witek *et al.*). Because the Nakai and Witek references address different problems and relate to significantly different subject matter, <u>there is no evidence of a suggestion, teaching, or motivation in the references to make the suggested combination</u>. The Applicants respectfully point out that combining prior art references without such evidence of a suggestion, teaching, or motivation simply takes the Applicants' disclosure as a blueprint for piecing together the prior art to defeat patentability, which is the essence of a forbidden <u>hindsight-based</u> obviousness analysis.

Even if a *prima facie* case of obviousness were properly established, the Applicants respectfully submit that neither the Nakai reference nor the Witek reference discloses an apparatus or method of computing a fast Fourier transform (FFT) in which <u>each</u>

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stage of the computation performs the same processing steps. For example, base claim 1 recites a method of computing an FFT in which each stage of the FFT computation performs the steps of storing a plurality of twiddle factors in a bit reversed order in a second memory, reading *a predetermined number R* of input butterfly data values of N first data values stored in a first memory, and performing *a radix R butterfly calculation* on the predetermined number R of input butterfly data values using at least one of the plurality of twiddle factors to generate *R output butterfly data values*. Similarly, base claim 5 recites an apparatus for calculating an FFT that includes a plurality of computation stages, each stage being operative to receive *a predetermined number R* of input butterfly data values for performing *a radix R butterfly calculation* to calculate *R output butterfly data values* using at least one twiddle factor value. In addition, base claim 8 recites a digital signal processing apparatus for performing an FFT calculation that includes a plurality of computation stages, each stage being operative to read *a predetermined number R* of input butterfly data values for performing *a radix R butterfly calculation*.

The notion of providing an apparatus and method of computing a fast Fourier transform (FFT) in which each stage of the FFT

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computation performs the same processing steps is described throughout the instant application, *e.g.*, see page 9, lines 1-8, page 12, lines 10-15, and Figs. 3 and 6, of the application. For example, Fig. 3 depicts a signal flow diagram of an illustrative FFT calculator stage **300**, which is operative to calculate an 8-point radix-2 FFT (see page 10, lines 8-10, of the application). Further, Fig. 6 depicts an 8-point radix-2 FFT signal flow diagram **600** including three stages **602**, **604**, and **606**.

As shown in Fig. 6, each one of the three stages **602**, **604**, and **606** is like the FFT calculator stage **300** (see Fig. 3), which performs the processing steps of reading a predetermined number R (*e.g.*, R = 2) of input butterfly data values of N (*e.g.*, N = 8) first data values, performing a radix R (R = 2) butterfly calculation on the predetermined number R (R = 2) of input butterfly data values to generate R (R = 2) output butterfly data values, and repeating the reading and performing steps N/R (*e.g.*, N/R = 8/2 = 4) x 2 times to complete the FFT computation for the respective stage using the *same* predetermined number R (*e.g.*, R = 2) each time these processing steps are performed, as recited in amended claims 1, 5, and 8.

In contrast, the Nakai and Witek references do not disclose apparatuses or methods of computing an FFT in which the stages of

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the FFT computation perform the same processing steps. For example, Nakai *et al.* disclose signal flow graphs showing radix-4x2 decimation-in-time calculations as examples of their FFT algorithm (see Figs. 4 and 13 of Nakai *et al.*). As shown in Fig. 4 of the Nakai reference, the stages 0-2 are different from one another, *e.g.*, stage 0 provides eight 4-point FFTs, stage 1 provides two 16-point FFTs, and stage 2 provides one 32-point FFT. Further, <u>the different stages 0-2 perform *different* processing steps</u> to compute the aforesaid eight 4-point FFTs, two 16-point FFTs, and one 32-point FFT.

As shown in Fig. 6 of the instant application, <u>each of the three stages of the FFT computation provides an 8-point radix-2 FFT</u>. Further, <u>each stage of the FFT computation is configured to perform the *same* processing steps</u> of reading a predetermined number R (*e.g.*, R = 2) of input butterfly data values of N (*e.g.*, N = 8) first data values, performing a radix R butterfly calculation on the predetermined number R of input butterfly data values to generate R output butterfly data values, and repeating the reading and performing steps N/R x 2 times to complete the FFT calculation for the stage, as recited in amended claims 1, 5, and 8.

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Important benefits can be achieved by providing the apparatus and method of computing an FFT, as recited in amended base claims 1, 5, and 8. For example, by allowing each stage of the FFT computation to perform the same processing steps, the number of overhead and control instructions that need to be executed in the computation is significantly reduced. Further, when the stride is unity in the third memory store operation of each stage, the R butterfly data values are stored contiguously in the third memory. Subsequent stages in an FFT processor operating according to base claims 1, 5, and 8 can therefore access contiguous memory locations when accessing the input data for each stage. As a result, the number of calculations needed for the memory operations is reduced, and the arithmetic that uses pointers or other memory accessing functions is simplified.

Because the Nakai and Witek references do not disclose an apparatus or method of computing an FFT in which each stage of the computation performs the same processing steps, neither the Nakai reference nor the Witek reference, taken alone or in combination, renders amended base claims 1, 5, and 8 and the claims dependent therefrom obvious. Accordingly, the Applicants respectfully submit that the rejections of the claims 1-8 under section 103 of the Patent Laws are unwarranted and should be withdrawn.

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In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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